

FIG. 1

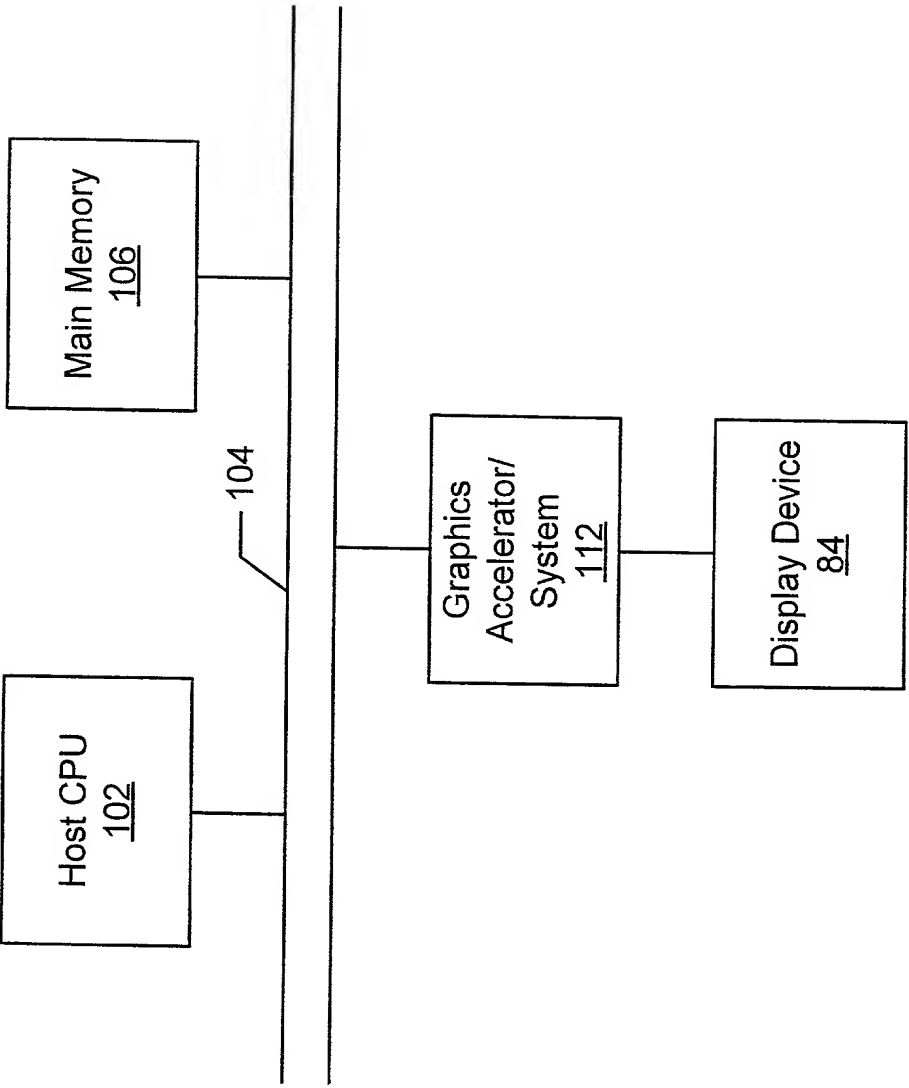


FIG. 2

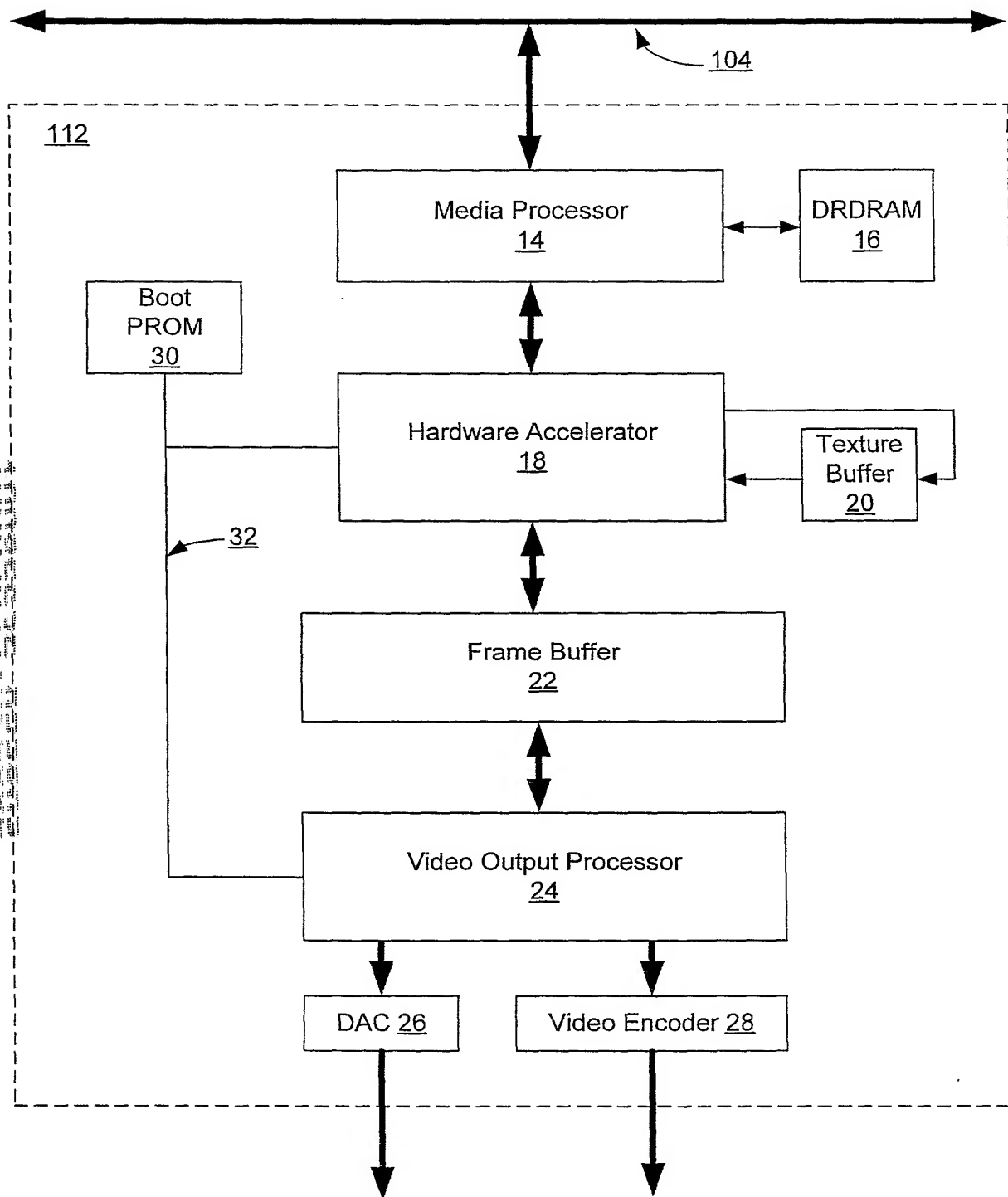


FIG. 3

FIG. 4 is a block diagram of a system 14, according to one embodiment. The system 14 includes a Host Interface 11, a Direct Port, an Accelerated Port, a Graphics Queue 148, a Geometry Data Preprocessor 150, a BIU 154, a RAC 156, a DRDRAM 16, an MPU1 152B, an MPU2 152A, and a Controller 160. The Host Interface 11 is connected to the Direct Port and the Accelerated Port. The Direct Port is connected to the BIU 154. The Accelerated Port is connected to the Graphics Queue 148 and the Geometry Data Preprocessor 150. The Graphics Queue 148 is connected to the Geometry Data Preprocessor 150. The Geometry Data Preprocessor 150 is connected to the BIU 154. The BIU 154 is connected to the RAC 156. The RAC 156 is connected to the DRDRAM 16. The BIU 154 is also connected to the MPU1 152B and the MPU2 152A. The MPU1 152B and the MPU2 152A are connected to the Controller 160. The Controller 160 is connected to the Accelerated Port.

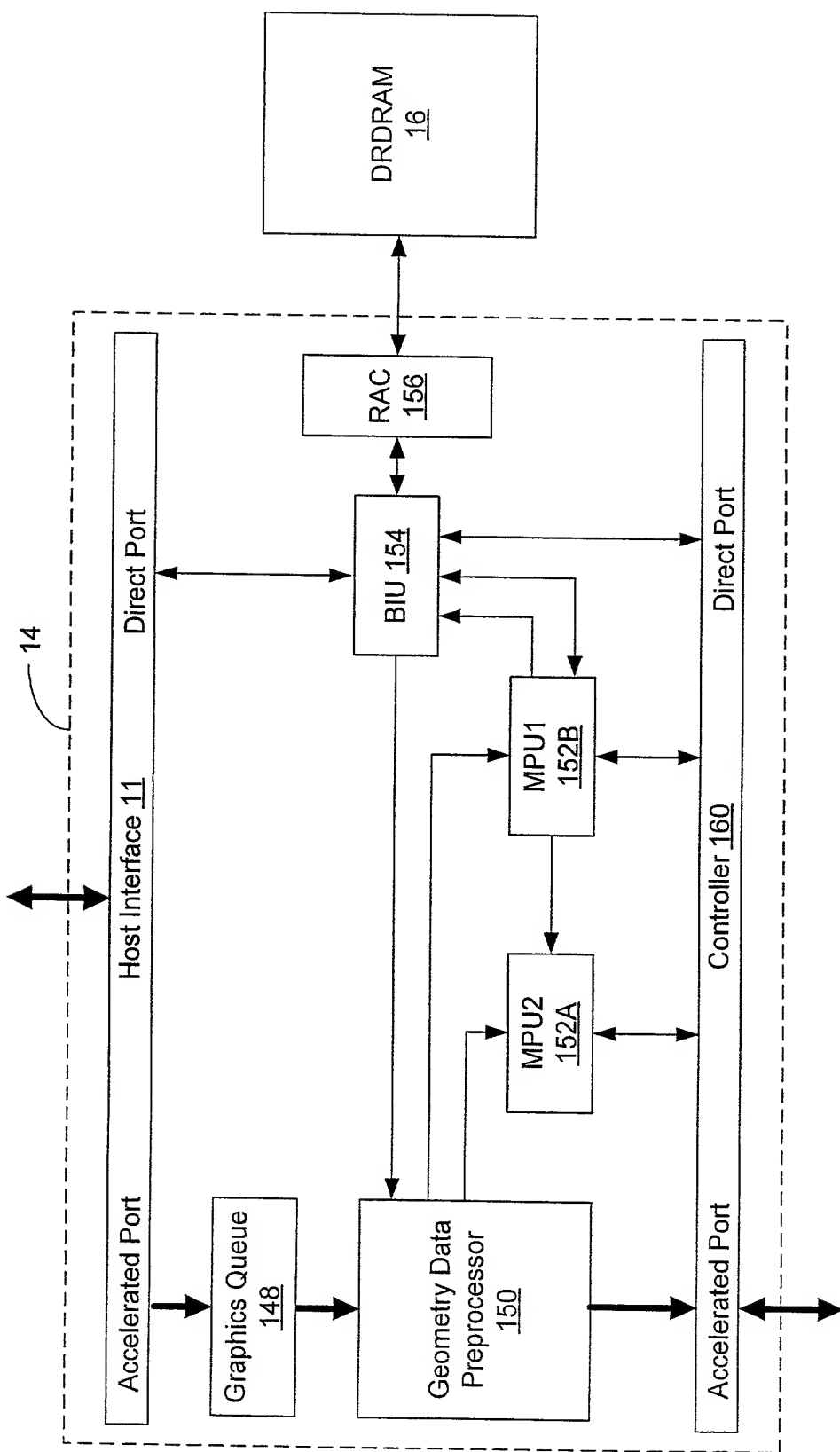


FIG. 4

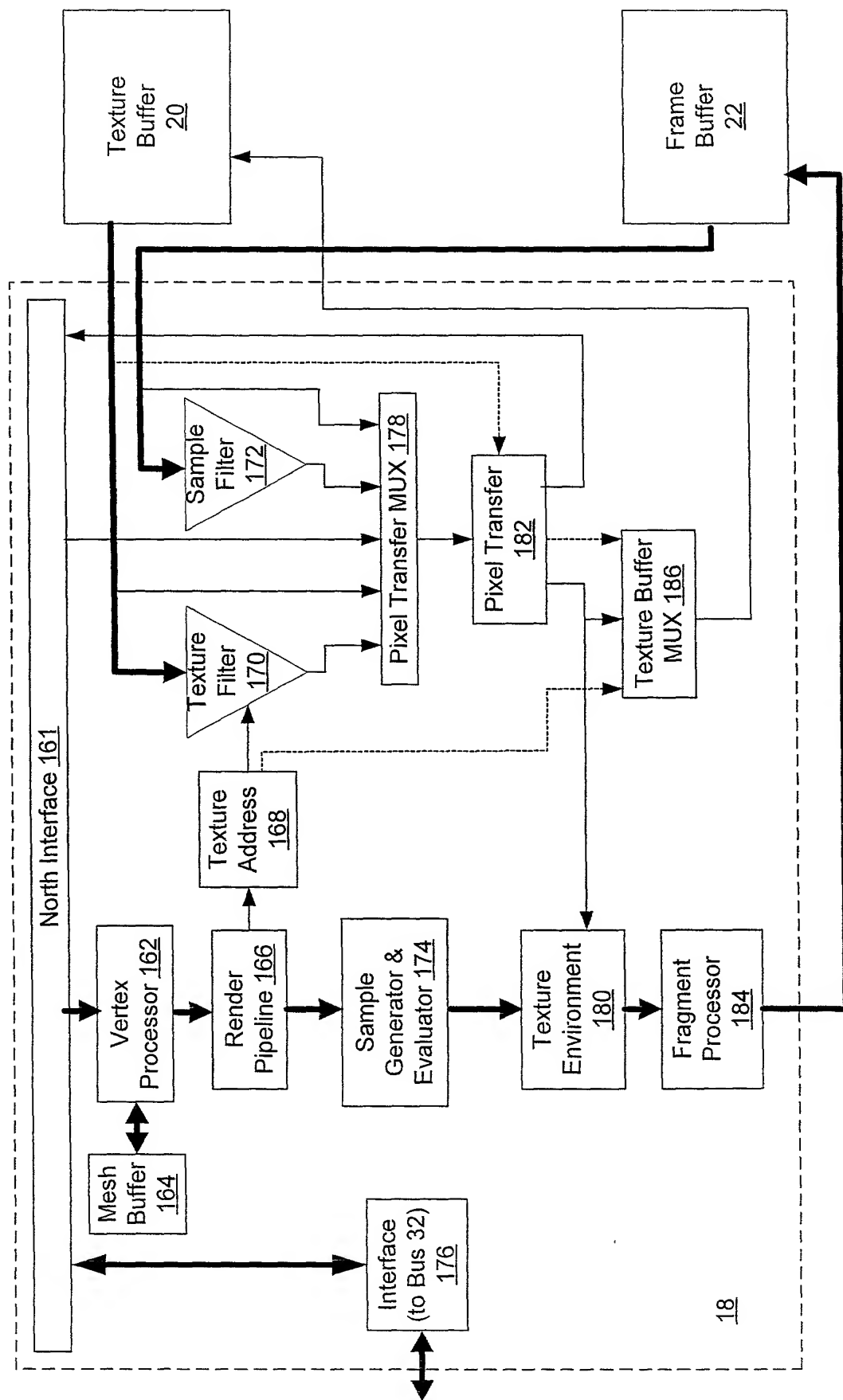


FIG. 5

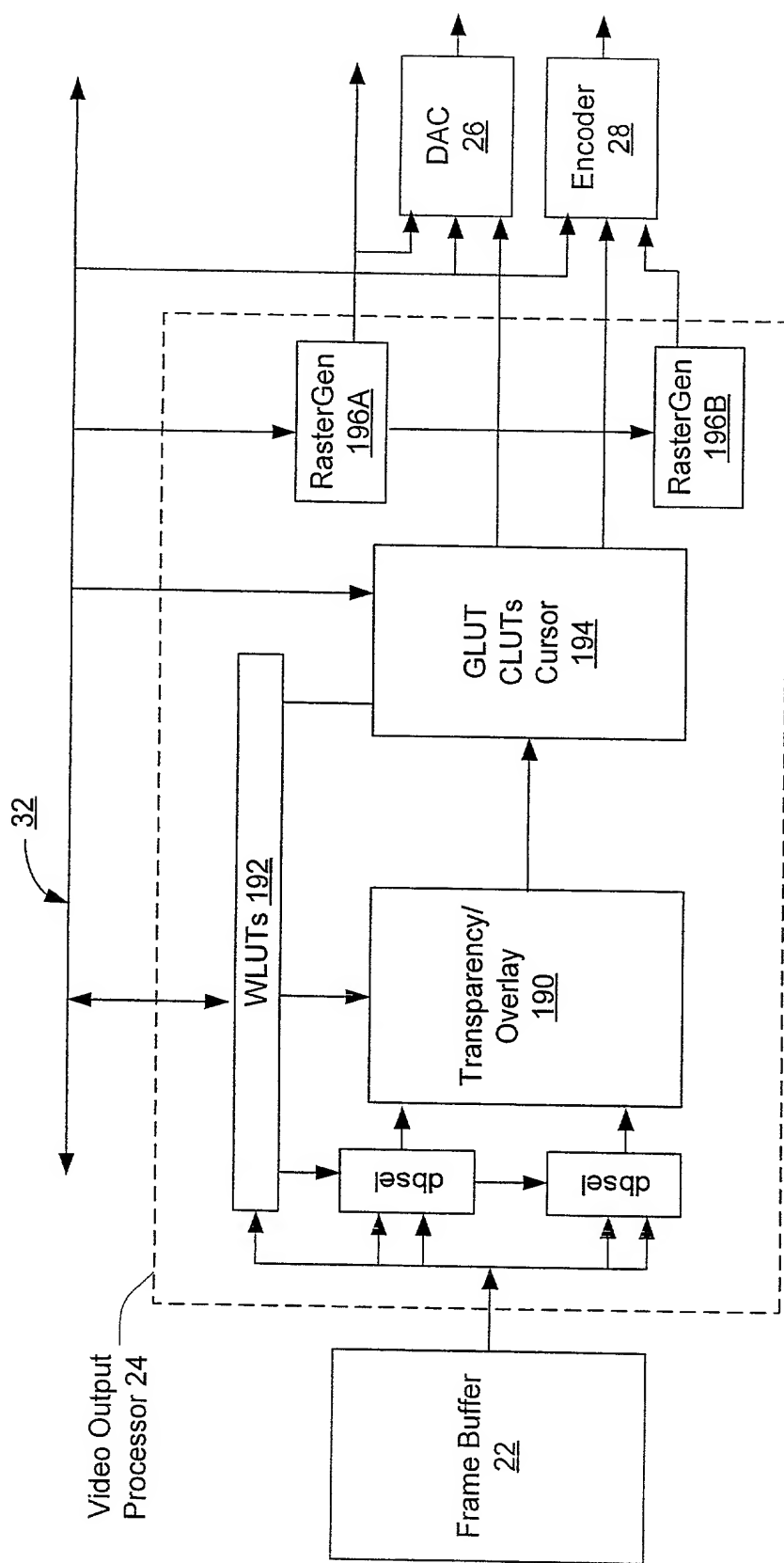


FIG. 6

FIG. 7 is a diagram illustrating a portion of a sample space. The diagram shows a grid of 2x2 tiles, each containing multiple samples (denoted as small circles). A triangle is overlaid on the grid, indicating a specific region of interest. The X and Y axes are shown, with the Y-axis pointing upwards and the X-axis pointing to the right.

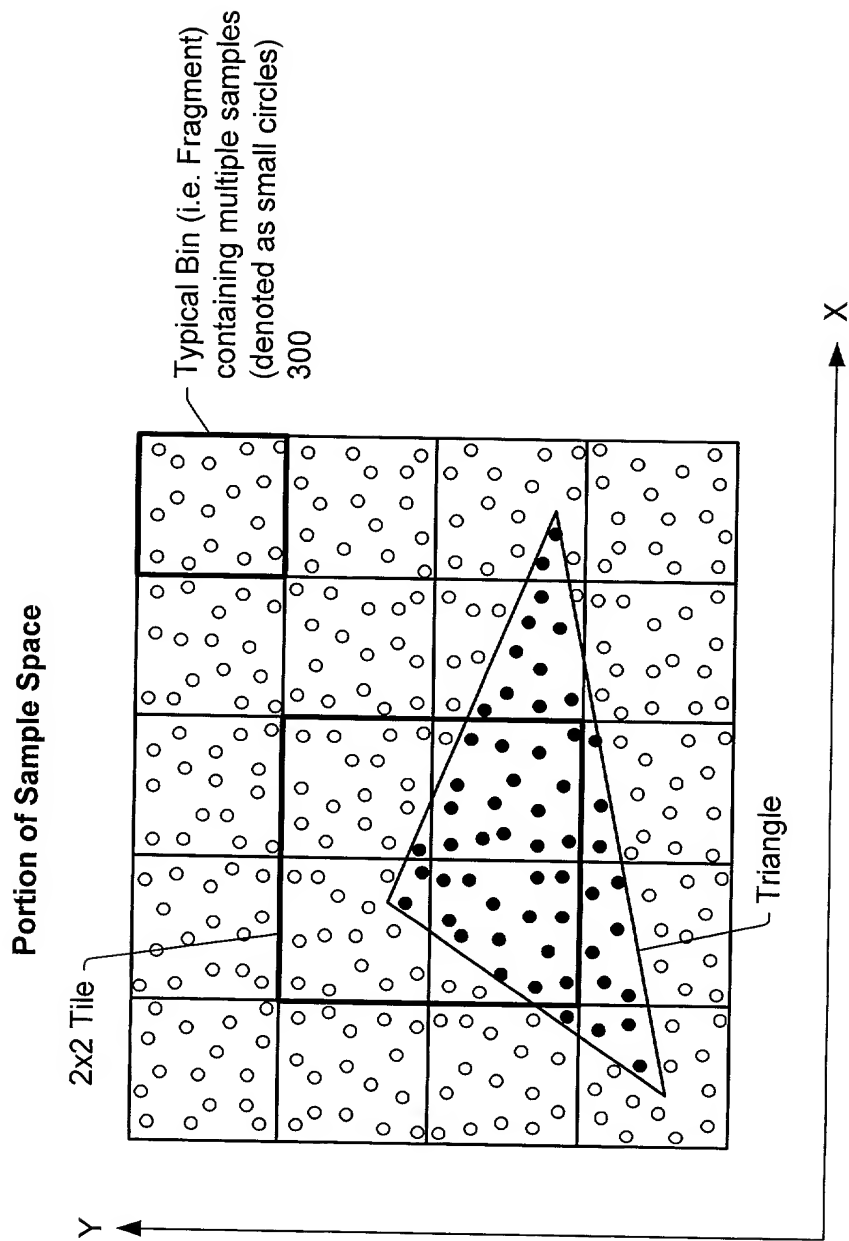


Fig. 7

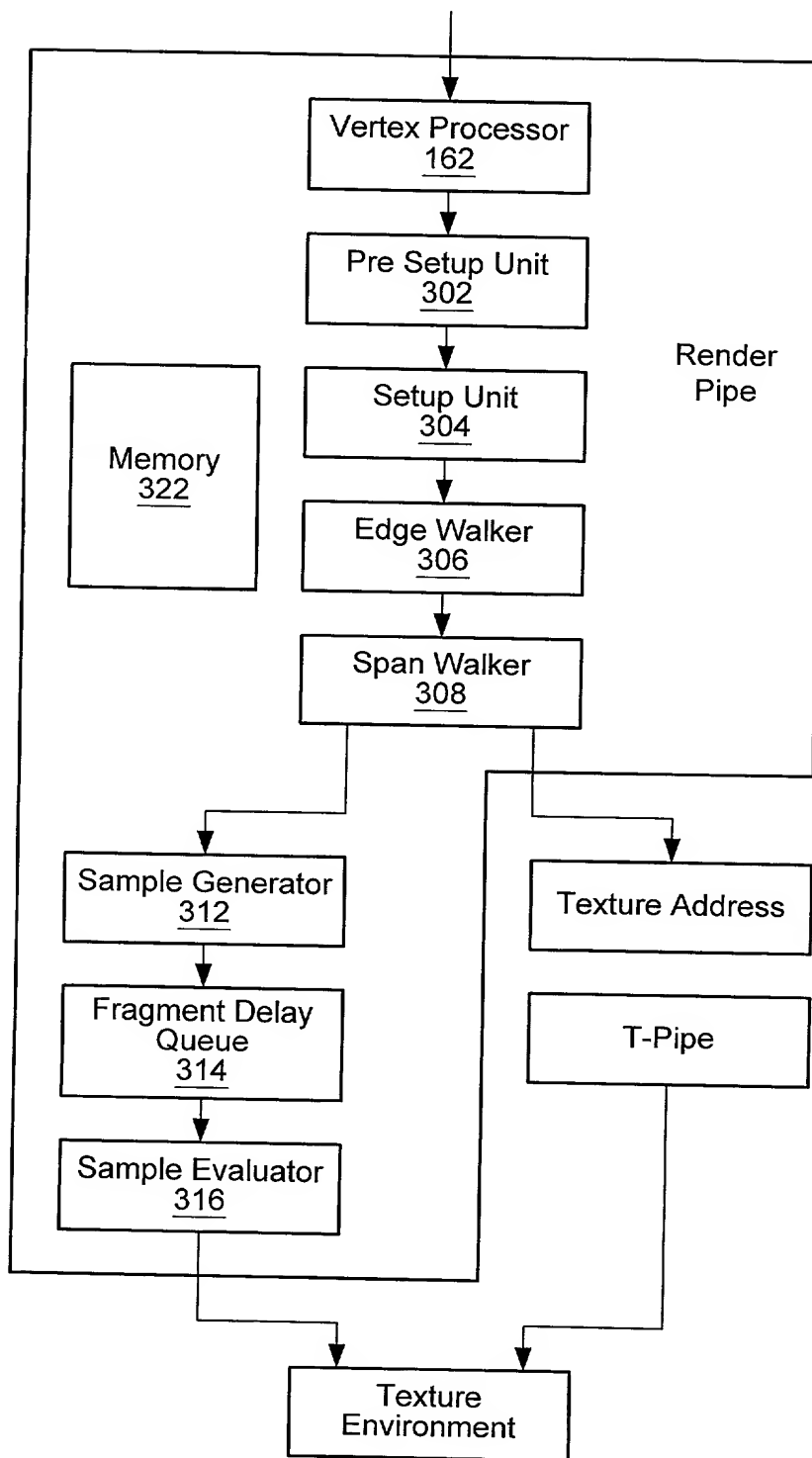
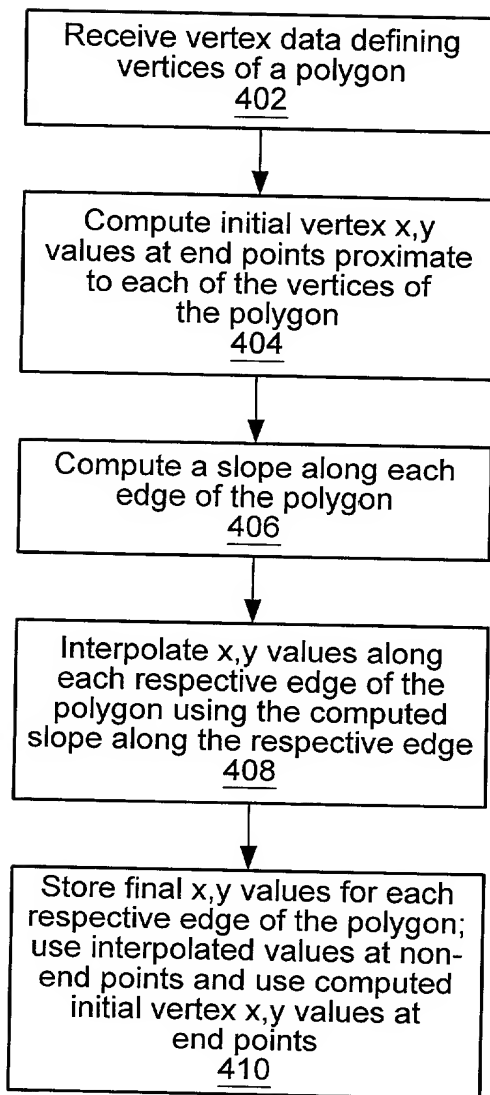


Fig. 8



*Fig. 9*

Pse, Psm, Pme are the initial edge intercepts

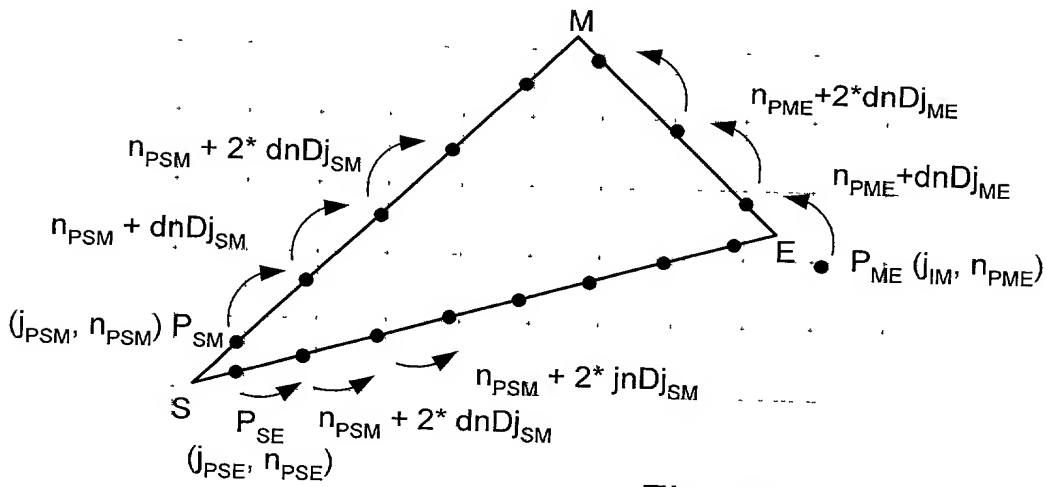
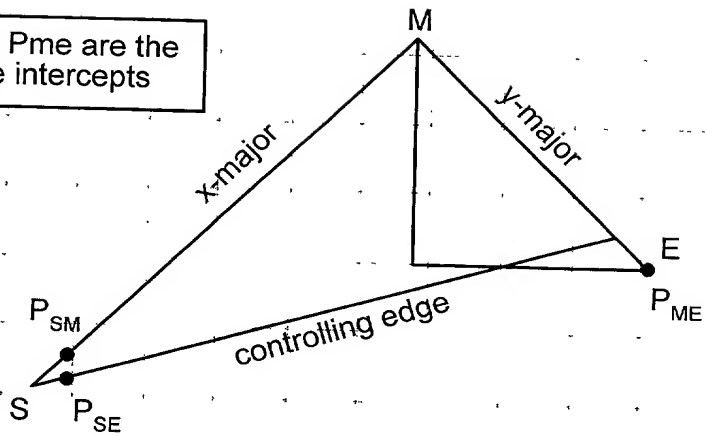


Fig. 10

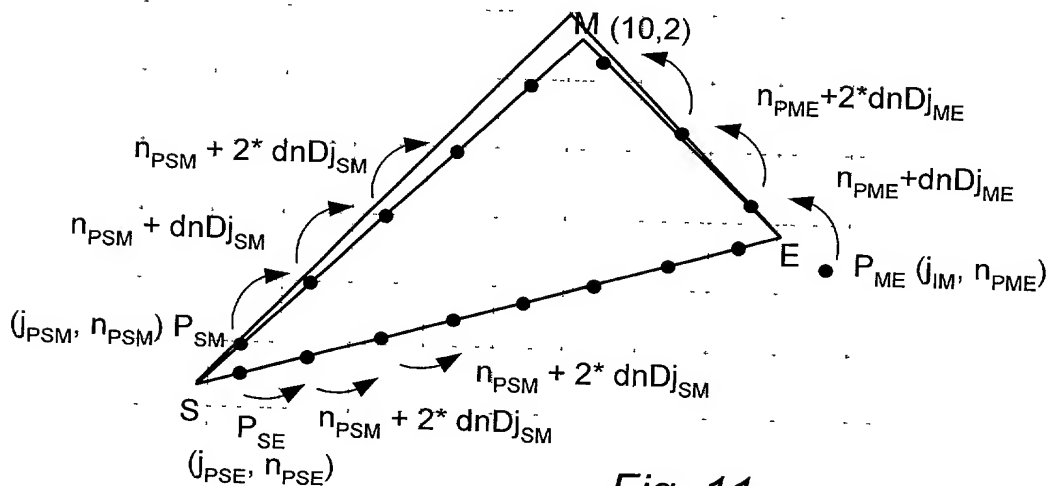


Fig. 11